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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,003	09/11/2003	Young-Bae Jung	21C-0085	5938

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CANTOR COLBURN LLP
55 Griffin Road South
Bloomfield, CT 06002

EXAMINER	
PARKER, KENNETH	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/660,003	Applicant(s) JUNG ET AL.	
	Examiner Kenneth A. Parker	Art Unit 2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-30 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) 1-22 is/are allowed.

6)☐ Claim(s) 23-30 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 23-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim 20020071086 in view of 20020080318, Yamate 20020080318, JP2000276073 and Asakura et al 6806938.

Kim et al discloses the device (and the associated method, the method being a mere recitation of the making of the element on the substrates, and then the assembing of the substrates), however Kim et al uses to layers for the data lines (the vertical lines), not the scan lines (the horizontal lines). Kim uses the scan and data metalizations for running the terminals of the data lines out further to aleviate the congestion (enable

connection and high resolution- page 2, paragraph 19) of the terminals (see cover figure). However, Kim et al only shows the method with the data lines, not the scan lines. The secondary references JP20020080318, Yamate and Asukara all show methods of aleviating the terminal congestion on the side of the scanning lines (Yamate figure 2), Asakura figure 16, and JP20020080318 in the cover figure. Therefore it would have been obvious to one of ordinary skill, in the device of Kim, to use the other of the data and scan line for alternating terminals to enable connection to higher resolution, the applicability being evidenced by the secondary references.

Detailed Discussion:

Regarding claim 23 the reference shows a method of manufacturing a liquid crystal display device, the method comprising: forming a first substrate including a display region and a peripheral region adjacent to the display region, the display region having a plurality of data lines, a plurality of scan lines, a plurality of pixels and a connecting part, each of the pixels having a switching device electrically coupled to one of the scan lines and one of the data lines (see figure 6b), the connecting part formed in the peripheral region adjacent to first ends the scan lines (in Kim it is the opposite- near the data lines), and the connecting part having a plurality of groups disposed in layers different from each other (see the bottom of the cover figure); combining the first substrate with a second substrate; and interposing a liquid crystal between the first and second substrates (required to make an LCD and therefore inherent).

Regarding claim 24 the reference shows the method of claim 23, wherein the first connecting part includes: a first group having a plurality of first connecting lines

formed from a same layer as the scan lines; and a second group having a plurality of second connecting lines formed from a same layer as the data lines (both layers are used).

Regarding claim 25 the reference shows the method of claim 24, wherein forming the first substrate includes: forming a first metal layer in the display region and the peripheral region; patterning the first metal layer to form the scan lines and gate electrodes branched from the scan lines on the display region and to form the first connecting lines electrically coupled to the first group of the scan lines (see figure 6a and 6b and the associated description, and patterning is inherent to forming the patterned shapes); forming an insulation layer, an active layer and a contact layer on the first substrate on which the scan lines, the gate electrodes and the first connecting lines are formed; patterning the active layer and the contact layer to form an active pattern and a contact pattern; forming a second metal layer on the first substrate on which the insulation layer, the active pattern and the contact pattern are formed (see figures 5a-c, and remember that the obviousness rejection applied reverses which connection is being doubled); and patterning the second metal layer to form the data lines, source electrodes branched from the data lines, (see figures 5a-c and 6a-b, and remember that the obviousness rejection applied reverses which connection is being doubled); and drain electrodes spaced apart from the source electrode on the display region, and to form the second connecting lines electrically coupled to a second group of the scan lines (see figures 5a-c, and 6a-b, and remember that the obviousness rejection applied reverses which connection is being doubled);.

Regarding claim 26 the reference shows the method of claim 25, wherein patterning the active layer and the contact layer further includes forming a double insulation layer on the peripheral region to be interposed between the insulation layer and the second connecting layer (see figure 5a);.

Regarding claim 27 the reference shows the method of claim 25, wherein patterning the active layer and the contact layer further includes forming a contact hole on the insulation layer, the active layer and the contact layer so that the contact hole exposes an end of the second group of the scan lines (see figures 5a-c, and remember that the obviousness rejection applied reverses which connection is being doubled);.

Regarding claim 28 the reference shows the method of claim 27, wherein the second connecting lines are electrically coupled to the second group of the scan lines (see figures 6a-c, and remember that the obviousness rejection applied reverses which connection is being doubled);.

Regarding claim 29 the reference shows the method of claim 24, wherein forming the first substrate includes: forming a first metal layer in the display region and the peripheral region; patterning the first metal layer to form the scan lines and gate electrodes branched from the scan lines on the display region, and to form the first connecting lines electrically coupled to first ends of the scan lines; forming an insulation layer, an active layer, a contact layer and a second metal layer on the first substrate on which the scan lines, the gate electrodes and the first connecting lines are formed; patterning the active layer, the contact layer and the second metal layer to form an active pattern and a contact pattern on each of the gate electrodes, to form the data

lines, source electrodes branched from the data lines, and drain electrodes spaced apart from the source electrodes on the display region, and to form the second connecting lines electrically coupled to second ends of the scan lines (see figures 5a-c and 6a-b) and remember that the obviousness rejection applied reverses which connection is being doubled);.

Regarding claim 30 the reference shows a substrate for a display device, the substrate comprising: a first substrate including a display region and a peripheral region adjacent to the display region (See cover figure), the display region having a plurality of pixels, a plurality of data lines and a plurality of scan lines (See cover figure), the peripheral region having a second peripheral region adjacent to first ends of the scan lines(See cover figure- left side and bottom); a driver section including a scan driver circuit and a data driver circuit, the scan driver circuit and the data driver circuit formed in the peripheral region, the scan driver circuit providing the scan lines with a scan driving signal, and the data driver circuit providing the data lines with a data signal (page 1, paragraph 14, and the definition of data lines is to receive data signals, and scan lines is to receive scan signals); and a first connecting part (the length between the edge of the display and the terminals) formed in the second peripheral region to be coupled to the first ends of the scan lines, the first connecting part including a plurality of groups, each of the groups disposed in first layers different from each other, the scan driving signal being applied to the first connecting part (here the reference shows the reverse, and the obviousness argument is applied to reverse which of the banks is doubled).

Allowable Subject Matter

Claims 1-22 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: The closest references, Kim and Asakura, fail to show the lines in both layers connecting as claimed. Yamate does show scanning lines in both layers, but fails to show both on the same side, as they run to different drive circuits.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth A. Parker whose telephone number is 571-272-2298. The examiner can normally be reached on M-F 10:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Kenneth A Parker/
Primary Examiner
Art Unit 2871